# R&E International A Subsidiary of Microchip Technology Inc.

**RE46C128** CMOS Ionization Smoke Detector ASIC with Interconnect Product Specification

#### **General Description**

The RE46C128 is low power CMOS ionization type smoke detector IC. With few external components this circuit will provide all the required features for an ionization type smoke detector.

An internal oscillator strobes power to the smoke detection circuitry for 10.5mS every 1.66 seconds to keep standby current to a minimum. A check for a low battery condition is performed every 40 seconds when in standby. The temporal horn pattern supports the NFPA 72 emergency evacuation signal.

An interconnect pin allows multiple detectors to be connected such that when one units alarms all units will sound.

Although this device was designed for smoke detection utilizing an ionization chamber it could be used in a variety of security applications.

Utilizing low power CMOS technology the RE46C128 was designed for use in smoke detectors that comply with Underwriters Laboratory Specification UL217 and UL268.

#### Features

- >1500V ESD Protection (HBM) on all Pins
- Guard Outputs for Ion Detector Input
- +/-0.75pA Detect Input Current
- Internal Reverse Battery Protection
- Low Quiescent Current Consumption (<6.5uA)
- Available in 16L PDIP or 16L N SOIC
- Internal Low Battery Detection
- Power Up Low Battery Test
- Interconnect up to 40 Detectors
- Compatible with Allegro A5364
- Available in Standard Packaging or RoHS Compliant Pb Free Packaging.

PITCOmguration								
N/C	1	16	GUARD2					
ю 🗌	2	15	DETECT					
LBADJ	3	14	GUARD1					
N/C	4	13	VSEN					
LED	5	12	OSCAP					
VDD	6	11	HS					
RBIAS	7	10	HB					
FEED	8	9	VSS					

Pin Configuration

#### ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNITS
Supply Voltage	$V_{DD}$	15	V
Input Voltage Range Except FEED, IO	V <sub>in</sub>	3 to V <sub>dd</sub> +.3	V
FEED Input Voltage Range	V <sub>infd</sub>	-10 to +22	V
IO Input Voltage Range	V <sub>io1</sub>	3 to 17	V
Reverse Battery Time	T <sub>RB</sub>	5	S
Input Current except FEED	l <sub>in</sub>	10	mA
Operating Temperature	T <sub>A</sub>	-10 to 60	°C
Storage Temperature	T <sub>STG</sub>	-55 to 125	°C
Maximum Junction Temperature	$T_{J}$	150	°C

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and operation at these conditions for extended periods may affect device reliability.

This product utilizes CMOS technology with static protection; however proper ESD prevention procedures should be used when handling this product. Damage can occur when exposed to extremely high static electrical charge.



## DC Electrical Characteristics at TA = 25°C, VDD=9V, OSCAP=.1uF, RBIAS=8.2M $\Omega$ , VSS=0V (unless otherwise noted)

		Test			Lin	nits	
Parameter	Symbol	Pin	Test Conditions	Min	Тур	Max	Units
Supply Voltage	V <sub>DD</sub>	6	Operating	6		12	V
Supply Current	I <sub>DD1</sub>	6	RBIAS=8.2MΩ, OSCAP=.1uF		5	6.5	uA
	I <sub>DD2</sub>	6	RBIAS=8.2MΩ, OSCAP=.1uF;Vdd=12V			9	uA
Input Voltage High	V <sub>IH1</sub>	8		6.2	4.5		V
	V <sub>IH2</sub>	2	No Local Alarm, IO as an Input	3			V
Input Voltage Low	V <sub>IL1</sub>	8			4.5	2.7	V
	V <sub>IL2</sub>	2	No Local Alarm, IO as an Input			1	V
Input Leakage Low	IL <sub>DET1</sub>	15	VDD=9V, DETECT=VSS, 0-40% RH			-0.75	pА
	IL <sub>DET2</sub>	15	VDD=9V, DETECT=VSS, 85% RH Note 1			-1.50	pА
	IL <sub>FD</sub>	8	FEED=-10V			-50	uA
Input Leakage High	IH <sub>DET1</sub>	15	VDD=9V, DETECT=VDD, 0-40% RH			0.75	pА
	IH <sub>DET2</sub>	15	VDD=9V, DETECT=VDD, 85% RH Note 1			1.50	pА
	IH <sub>FD</sub>	8	FEED=22V			50	uA
	I <sub>IOL2</sub>	2	No Alarm, Vio=17V			150	uA
Output Off Leakage High	I <sub>IOHZ</sub>	5	Outputs Off			1	uA
Output High Voltage	V <sub>OH1</sub>	10,11	IOH=-16mA, VDD=7.2V	6.3			V
Output Low Voltage	V <sub>OL1</sub>	10,11	IOL=16mA, VDD=7.2V			.9	V
	V <sub>OL3</sub>	5	IOL=10mA, VDD=7.2V			1	V
Output Current	I <sub>IOL1</sub>	2	No Alarm, Vio=Vdd-2V	25		60	uA
	I <sub>IOH1</sub>	2	Alarm, Vio=Vdd-2V or Vio=0V	-4		-16	mA
	I <sub>IODMP</sub>	2	At Conclusion of Local Alarm or Test, Vio=1V	5			mA
Low Battery Voltage	V <sub>LB</sub>	6	T <sub>A</sub> =-10 to 60°C, Note 3	7.2	7.5	7.8	V
Internal Sensitivity Set Voltage	V <sub>SET1</sub>	13		48.5	50	51.5	$%V_{DD}$
	V <sub>SET2</sub>	3			65.5		%V <sub>DD</sub>



#### **DC Electrical Characteristics – Continued**

		Test		Limits			
Parameter	Symbol	Pin	Test Conditions	Min	Тур	Max	Units
Offset Voltage	VG <sub>OS1</sub>	14,15	Guard Amplifier	-50		50	mV
	VG <sub>OS2</sub>	15,16	Guard Amplifier	-50		50	mV
	VG <sub>OS3</sub>	13,15	Smoke Comparator	-50		50	mV
Common Mode Voltage	V <sub>CM1</sub>	14,15	Guard Amplifier, Note 2	2		V <sub>DD</sub> 5	V
	V <sub>CM2</sub>	13,15	Smoke Comparator, Note 2	.5		V <sub>DD</sub> -2	V
Output Impedance	Z <sub>OUT</sub>	14,16	Guard Amplifier Outputs, Note 2		10		kΩ
Hysteresis	V <sub>HYS</sub>	13	No Alarm to Alarm Condition	90	130	170	mV

Note 1: Sample test only.

Note 2: Not 100% production tested.

Note 3: Production test at room with temperature guardbanded limits.

## AC Electrical Characteristics at TA = 25°C, VDD=9V, OSCAP=.1uF, RBIAS=8.2M $\Omega$ , VSS=0V (unless otherwise noted)

		Test		Limits			
Parameter	Symbol	Pin	Test Conditions	Min	Тур	Max	Units
Oscillator Period	T <sub>PER1</sub>	12	No Alarm Condition	1.34	1.67	2	S
	T <sub>PER2</sub>	12	Alarm Condition	37.5	41.5	45.8	mS
Oscillator Pulse Width	T <sub>PW</sub>	5	Operating	9.4	10.5	12.9	mS
LED On Time	T <sub>LON</sub>	5	Operating	9.4	10.5	12.9	mS
LED Off Time	T <sub>LOF1</sub>	5	Standby, No Alarm	32	40	48	S
	T <sub>LOF2</sub>	5	Alarm Condition	.8	1	1.2	S
	T <sub>LOF3</sub>	5	Timer Mode, No Alarm	8	10	12	S
Horn On Time	T <sub>HON1</sub>	10,11	Operating, Alarm Condition, Note 4	450	500	550	mS
	T <sub>HON2</sub>	10,11	Low Battery, No Alarm	9.4	10.5	12.9	mS
Horn Off Time	T <sub>HOF1</sub>	10,11	Operating, Alarm Condition, Note 4	450	500	550	mS
	T <sub>HOF2</sub>	10,11	Operating, Alarm Condition, Note 4	1.35	1.5	1.65	S
	T <sub>HOF3</sub>	10,11	Low Battery, No Alarm	32	40	48	S
IO Charge Dump Duration	TIODMP	2	At Conclusion of Local Alarm or Test	1.34	1.67	2.0	S
IO Delay	T <sub>IODLY1</sub>	2	From Start of Local Alarm to IO Active		3		S
IO Filter	T <sub>IOFILT</sub>	2	IO pulse width guaranteed to be filtered. IO as Input, No Local Alarm			450	mS
Remote Alarm Delay	T <sub>IODLY2</sub>	2	No Local Alarm, IO as input, From IO active to Horn Active	.450		2.2	S

Note 4 – See timing diagram for horn temporal pattern.

All timing except for  $T_{\text{PER}}$  and  $T_{\text{PW}}$  are guaranteed by functional tests.

**CMOS Ionization Smoke Detector ASIC with Interconnect** Product Specification



**R&E International** A Subsidiary of Microchip Technology Inc.

#### RE46c128 Functional Block Diagram

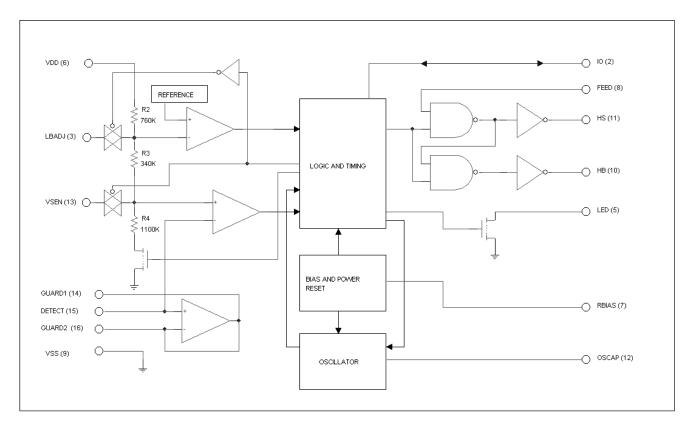


Figure 1



### **DEVICE DESCRIPTION and APPLICATION NOTES**

<u>Internal Timing</u> – With external components as indicated on the application drawing the period of the oscillator is nominally 1.67 seconds in standby. Every 1.66 seconds the detection circuitry is powered up for 10.5mS and the status of the smoke comparator is latched. In addition every 40 seconds the LED driver is turned on for 10.5mS and the status of the low battery comparator is latched. The smoke comparator status is not checked during the low battery test, during the low battery horn warning chirp, or when the horn is on due to an alarm condition.

If an alarm condition is detected the oscillator period increases to 41.5mS.

Due to the low currents used in the oscillator the capacitor on pin 12 should be a low leakage type. Oscillator accuracy will depend mainly on the tolerance of the RBIAS resistor and OSCAP capacitor.

<u>Smoke Detection Circuit</u> – The smoke comparator compares the ionization chamber voltage to a voltage derived from a resistor divider across VDD. This divider voltage is available externally on pin 13 (VSEN). When smoke is detected this voltage is internally increased by 130mV nominal to provide hysteresis and make the detector less sensitive to false triggering.

Pin 13 (VSEN) can be used to modify the internal set point for the smoke comparator by use of external resistors to VDD or VSS. Nominal values for the internal resistor divider are indicated on the block diagram. These internal resistor values can vary by up to ±20% but the resistor matching should be <2% on any one device. Transmission switches on VSEN and LBADJ prevent any interaction from the external adjustment resistors.

The guard amplifier and outputs are always active and will be within 50mV of the DETECT input to reduce surface leakage. The guard outputs also allow for measurement of the DETECT input without loading the ionization chamber.

<u>Low Battery Detection</u> - An internal reference is compared to the voltage divided VDD supply. The battery can be checked under load via the LED low side driver output since low battery status is latched at the end of the 10.5mS LED pulse. Pin 3 (LBADJ) can be used to modify the low battery set point by placing a resistor to VDD or VSS. Transmission switches on VSEN and LBADJ prevent any interaction from external adjustment resistance.

<u>LED Pulse</u> – The LED is pulsed on for 10.5mS every 40S in standby. In alarm the LED is pulsed on for 10.5mS every 1S.

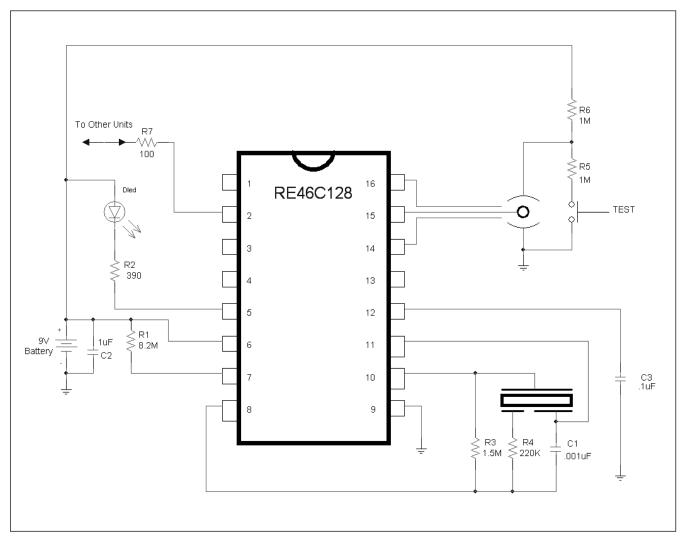
<u>Interconnect</u> – Pin 2 (IO) provides the capability to common many detectors in a single system. If a single unit goes into alarm the IO pin is driven high. This high signal causes the interconnected units to alarm. The LED flashes every 1S for 10.5mS on the signaling unit and is inhibited on the units that are in alarm due to the IO signal. An internal sink device on the IO pin helps to discharge the interconnect line. This charge dump device is active for 1 clock cycle after the unit exits the alarm condition (1.67S).

The interconnect input has a 1000mS nominal digital filter. This allows for interconnection to other types of alarms (carbon monoxide for example) that may have a pulsed interconnect signal.

<u>Testing</u> – At power up all internal registers are reset. The low battery set point can be tested at power up by holding FEED and OSCAP low at power up. HB will change state as VDD passes through the low battery set point. By holding pin 12 (OSCAP) low the internal power strobe is active. Functional testing can be accelerated by driving pin 12 with a 4 kHz square wave however the 10.5mS strobe period must be maintained for proper operation of the analog circuitry. Please refer to the timing diagrams.



A Subsidiary of Microchip Technology Inc.



#### RE46c128 Typical Application

Figure 2

Notes:

Pins 1 and 4 are not used.

External resistors on pin 13 can be used to adjust the alarm threshold.

R3, R4 and C1 are typical values and may be adjusted to maximize sound pressure.

C2 should be located as close as possible to the device power pins.

Route the pin 8 PC board trace away from pin 7 to avoid signal coupling.

**CMOS Ionization Smoke Detector ASIC with Interconnect** Product Specification



			Timing Diagra	m		
	Standby Mode; No Low	Battery; No Alarm	Alarm; No Low Battery	Alarm; Low Battery	No Alarm; Low Battery	<b>&gt;</b>
Oscillator	Pin 15 > Pin 13		Pin 13 > Pin 15; 130mV Level Shift o		15 > Pin 13	N
Internal Clock	1.67S 10.5ms		10000000000000000000000000000000000000		<u>.</u>	
LED	<	→ 		<b>_</b>	1	
Sample Smoke						
Horn			See Figure Below for Complete Horn Cycle		Low Battery Warning Chirp	
IO (Pin 2) as Outpu	ut	Timing not same scale	→			
IO Charge Dump						
IO ( Pin 2) as Input	T <sub>iofilt</sub>	→ ► 	► T <sub>100.12</sub>	LED supressed in remote alarm mod	e	
Horn Start of horn te	emporal pattern is not synchroni	zed to an external alarm		Horn pattern not self completing for external a	alarm,see timing below for complete horn cycle	
Internal Clock						
2. Low battery warr	mpled when the horn is ning chirp is suppressed only in local alarm, inac	in local or remote alar	elf completing in local alarm. m			
	T,	on1 T <sub>HOF1</sub>	T <sub>HOF2</sub>			

Complete Temporal Horn Pattern

### RE46C128

**CMOS Ionization Smoke Detector ASIC with Interconnect** Product Specification



R&E International

A Subsidiary of Microchip Technology Inc.

Information contained in this publication regarding device applications and the like is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION, INCLUDING BUT NOT LIMITED TO ITS CONDITION, QUALITY, PERFORMANCE, MERCHANTABILITY OR FITNESS FOR PURPOSE. Microchip disclaims all liability arising from this information and its use. Use of Microchip devices in life support and/or safety applications is entirely at the buyer's risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights.

#### Trademarks

The Microchip name and logo, the Microchip logo, Accuron, dsPIC, KEELOQ, KEELOQ logo, MPLAB, PIC, PICmicro, PICSTART, rfPIC, SmartShunt and UNI/O are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

FilterLab, Hampshire, Linear Active Thermistor, MXDEV, MXLAB, SEEVAL, SmartSensor and The Embedded Control Solutions Company are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Analog-for-the-Digital Age, Application Maestro, CodeGuard, dsPICDEM, dsPICDEM.net, dsPICworks, dsSPEAK, ECAN, ECONOMONITOR, FanSense, In-Circuit Serial Programming, ICSP, ICEPIC, Mindi, MiWi, MPASM, MPLAB Certified logo, MPLIB, MPLINK, mTouch, nanoWatt XLP, PICkit, PICDEM, PICDEM.net, PICtail, PIC<sup>32</sup> logo, PowerCal, PowerInfo, PowerMate, PowerTool, REAL ICE, rfLAB, Select Mode, Total Endurance, TSHARC, WiperLock and ZENA are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

SQTP is a service mark of Microchip Technology Incorporated in the U.S.A.

All other trademarks mentioned herein are property of their respective companies.

© 2009, Microchip Technology Incorporated, Printed in the U.S.A., All Rights Reserved.

Printed on recycled paper.

### QUALITY MANAGEMENT SYSTEM CERTIFIED BY DNV ISO/TS 16949:2002

Microchip received ISO/TS-16949:2002 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.